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**********************************************************
   29818 Tue Aug 11 14:42:14 2015
new/usr/src/uts/intel/sys/x86_archext.h
6116 FMT_CPUID_AMD_ECX is wrong
**********************************************************
```

```
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 */

#ifndef _SYS_X86_ARCHEXT_H
#define _SYS_X86_ARCHEXT_H

#if !defined(_ASM)
#include <sys/regset.h>
#include <sys/processor.h>
#include <vm/seg_enum.h>
#include <vm/page.h>
#endif  /* _ASM */

#ifdef __cplusplus
extern "C" {
#endif

/*
 * cpuid instruction feature flags in %edx (standard function 1)
 */

#define CPUID_INTC_EDX_FPU      0x00000001      /* x87 fpu present */
#define CPUID_INTC_EDX_VME      0x00000002      /* virtual-8086 extension */
#define CPUID_INTC_EDX_DE       0x00000004      /* debugging extensions */
#define CPUID_INTC_EDX_PSE      0x00000008      /* page size extension */
#define CPUID_INTC_EDX_TSC      0x00000010      /* time stamp counter */
#define CPUID_INTC_EDX_MSR      0x00000020      /* rdmsr and wrmsr */
#define CPUID_INTC_EDX_PAE      0x00000040      /* physical addr extension */
```



```
#define CPUID_INTC_EDX_MCE      0x00000080      /* machine check exception */
#define CPUID_INTC_EDX_CX8      0x00000100      /* cmpxchg8b instruction */
#define CPUID_INTC_EDX_APIC     0x00000200      /* local APIC */
                                                /* 0x400 - reserved */
#define CPUID_INTC_EDX_SEP      0x00000800      /* sysenter and sysexit */
#define CPUID_INTC_EDX_MTRR     0x00001000      /* memory type range reg */
#define CPUID_INTC_EDX_PGE      0x00002000      /* page global enable */
#define CPUID_INTC_EDX_MCA      0x00004000      /* machine check arch */
#define CPUID_INTC_EDX_CMOV     0x00008000      /* conditional move insns */
#define CPUID_INTC_EDX_PAT      0x00010000      /* page attribute table */
#define CPUID_INTC_EDX_PSE36    0x00020000      /* 36-bit pagesize extension */
#define CPUID_INTC_EDX_PSN      0x00040000      /* processor serial number */
#define CPUID_INTC_EDX_CLFSH    0x00080000      /* clflush instruction */
                                                /* 0x100000 - reserved */
#define CPUID_INTC_EDX_DS       0x00200000      /* debug store exists */
#define CPUID_INTC_EDX_ACPI     0x00400000      /* monitoring + clock ctrl */
#define CPUID_INTC_EDX_MMX      0x00800000      /* MMX instructions */
#define CPUID_INTC_EDX_FXSR     0x01000000      /* fxsave and fxrstor */
#define CPUID_INTC_EDX_SSE      0x02000000      /* streaming SIMD extensions */
#define CPUID_INTC_EDX_SSE2     0x04000000      /* SSE extensions */
#define CPUID_INTC_EDX_SS       0x08000000      /* self-snoop */
#define CPUID_INTC_EDX_HTT      0x10000000      /* Hyper Thread Technology */
#define CPUID_INTC_EDX_TM       0x20000000      /* thermal monitoring */
#define CPUID_INTC_EDX_IA64     0x40000000      /* Itanium emulating IA32 */
#define CPUID_INTC_EDX_PBE      0x80000000      /* Pending Break Enable */

#define FMT_CPUID_INTC_EDX                                              \
        "\20"                                                           \
        "\40pbe\37ia64\36tm\35htt\34ss\33sse2\32sse\31fxsr"     \
        "\30mmx\27acpi\26ds\24clfsh\23psn\22pse36\21pat"        \
        "\20cmov\17mca\16pge\15mtrr\14sep\12apic\11cx8"         \
        "\10mce\7pae\6msr\5tsc\4pse\3de\2vme\1fpu"

/*
 * cpuid instruction feature flags in %ecx (standard function 1)
 */

#define CPUID_INTC_ECX_SSE3     0x00000001      /* Yet more SSE extensions */
#define CPUID_INTC_ECX_PCLMULQDQ 0x00000002     /* PCLMULQDQ insn */
                                                /* 0x00000004 - reserved */
#define CPUID_INTC_ECX_MON      0x00000008      /* MONITOR/MWAIT */
#define CPUID_INTC_ECX_DSCPL    0x00000010      /* CPL-qualified debug store */
#define CPUID_INTC_ECX_VMX      0x00000020      /* Hardware VM extensions */
#define CPUID_INTC_ECX_SMX      0x00000040      /* Secure mode extensions */
#define CPUID_INTC_ECX_EST      0x00000080      /* enhanced SpeedStep */
#define CPUID_INTC_ECX_TM2      0x00000100      /* thermal monitoring */
#define CPUID_INTC_ECX_SSSE3    0x00000200      /* Supplemental SSE3 insns */
#define CPUID_INTC_ECX_CID      0x00000400      /* L1 context ID */
                                                /* 0x00000800 - reserved */
#define CPUID_INTC_ECX_FMA      0x00001000      /* Fused Multiply Add */
#define CPUID_INTC_ECX_CX16     0x00002000      /* cmpxchg16 */
#define CPUID_INTC_ECX_ETPRD    0x00004000      /* extended task pri messages */
                                                /* 0x00008000 - reserved */
                                                /* 0x00010000 - reserved */
                                                /* 0x00020000 - reserved */
#define CPUID_INTC_ECX_DCA      0x00040000      /* direct cache access */
#define CPUID_INTC_ECX_SSE4_1   0x00080000      /* SSE4.1 insns */
#define CPUID_INTC_ECX_SSE4_2   0x00100000      /* SSE4.2 insns */
#define CPUID_INTC_ECX_X2APIC   0x00200000      /* x2APIC */
#define CPUID_INTC_ECX_MOVBE    0x00400000      /* MOVBE insn */
#define CPUID_INTC_ECX_POPCNT   0x00800000      /* POPCNT insn */
#define CPUID_INTC_ECX_AES      0x02000000      /* AES insns */
#define CPUID_INTC_ECX_XSAVE    0x04000000      /* XSAVE/XRESTOR insns */
#define CPUID_INTC_ECX_OSXSAVE  0x08000000      /* OS supports XSAVE insns */
#define CPUID_INTC_ECX_AVX      0x10000000      /* AVX supported */
#define CPUID_INTC_ECX_F16C     0x20000000      /* F16C supported */
```

```
#define CPUID_INTC_ECX_RDRAND   0x40000000      /* RDRAND supported */
#define CPUID_INTC_ECX_HV       0x80000000      /* Hypervisor */

#define FMT_CPUID_INTC_ECX                                          \
        "\20"                                                       \
        "\37rdrand\36f16c\35avx\34osxsav\33xsave"                   \
        "\32aes"                                                    \
        "\30popcnt\27movbe\26x2apic\25sse4.2\24sse4.1\23dca"        \
        "\20\17etprd\16cx16\13cid\12ssse3\11tm2"                    \
        "\10est\7smx\6vmx\5dscpl\4mon\2pclmulqdq\1sse3"

/*
 * cpuid instruction feature flags in %edx (extended function 0x80000001)
 */

#define CPUID_AMD_EDX_FPU       0x00000001      /* x87 fpu present */
#define CPUID_AMD_EDX_VME       0x00000002      /* virtual-8086 extension */
#define CPUID_AMD_EDX_DE        0x00000004      /* debugging extensions */
#define CPUID_AMD_EDX_PSE       0x00000008      /* page size extensions */
#define CPUID_AMD_EDX_TSC       0x00000010      /* time stamp counter */
#define CPUID_AMD_EDX_MSR       0x00000020      /* rdmsr and wrmsr */
#define CPUID_AMD_EDX_PAE       0x00000040      /* physical addr extension */
#define CPUID_AMD_EDX_MCE       0x00000080      /* machine check exception */
#define CPUID_AMD_EDX_CX8       0x00000100      /* cmpxchg8b instruction */
#define CPUID_AMD_EDX_APIC      0x00000200      /* local APIC */
                                                /* 0x00000400 - sysc on K6m6 */
#define CPUID_AMD_EDX_SYSC      0x00000800      /* AMD: syscall and sysret */
#define CPUID_AMD_EDX_MTRR      0x00001000      /* memory type and range reg */
#define CPUID_AMD_EDX_PGE       0x00002000      /* page global enable */
#define CPUID_AMD_EDX_MCA       0x00004000      /* machine check arch */
#define CPUID_AMD_EDX_CMOV      0x00008000      /* conditional move insns */
#define CPUID_AMD_EDX_PAT       0x00010000      /* K7: page attribute table */
#define CPUID_AMD_EDX_FCMOV     0x00010000      /* FCMOVcc etc. */
#define CPUID_AMD_EDX_PSE36     0x00020000      /* 36-bit pagesize extension */
                                /* 0x00040000 - reserved */
                                /* 0x00080000 - reserved */
#define CPUID_AMD_EDX_NX        0x00100000      /* AMD: no-execute page prot */
                                /* 0x00200000 - reserved */
#define CPUID_AMD_EDX_MMXamd    0x00400000      /* AMD: MMX extensions */
#define CPUID_AMD_EDX_MMX       0x00800000      /* MMX instructions */
#define CPUID_AMD_EDX_FXSR      0x01000000      /* fxsave and fxrstor */
#define CPUID_AMD_EDX_FFXSR     0x02000000      /* fast fxsave/fxrstor */
#define CPUID_AMD_EDX_1GPG      0x04000000      /* 1GB page */
#define CPUID_AMD_EDX_TSCP      0x08000000      /* rdtscp instruction */
                                /* 0x10000000 - reserved */
#define CPUID_AMD_EDX_LM        0x20000000      /* AMD: long mode */
#define CPUID_AMD_EDX_3DNowx    0x40000000      /* AMD: extensions to 3DNow! */
#define CPUID_AMD_EDX_3DNow     0x80000000      /* AMD: 3DNow! instructions */

#define FMT_CPUID_AMD_EDX                                           \
        "\20"                                                       \
        "\40a3d\37a3d+\36lm\34tscp\32ffxsr\31fxsr"                  \
        "\30mmx\27mmxext\25nx\22pse\21pat"                          \
        "\20cmov\17mca\16pge\15mtrr\14syscall\12apic\11cx8"         \
        "\10mce\7pae\6msr\5tsc\4pse\3de\2vme\1fpu"

#define CPUID_AMD_ECX_AHF64     0x00000001      /* LAHF and SAHF in long mode */
#define CPUID_AMD_ECX_CMP_LGCY  0x00000002      /* AMD: multicore chip */
#define CPUID_AMD_ECX_SVM       0x00000004      /* AMD: secure VM */
#define CPUID_AMD_ECX_EAS       0x00000008      /* extended apic space */
#define CPUID_AMD_ECX_CR8D      0x00000010      /* AMD: 32-bit mov %cr8 */
#define CPUID_AMD_ECX_LZCNT     0x00000020      /* AMD: LZCNT insn */
#define CPUID_AMD_ECX_SSE4A     0x00000040      /* AMD: SSE4A insns */
#define CPUID_AMD_ECX_MAS       0x00000080      /* AMD: MisAlignSse mnode */
#define CPUID_AMD_ECX_3DNP      0x00000100      /* AMD: 3DNowPrefectch */
#define CPUID_AMD_ECX_OSVW      0x00000200      /* AMD: OSVW */
```



```
#define CPUID_AMD_ECX_IBS       0x00000400      /* AMD: IBS */
#define CPUID_AMD_ECX_SSE5      0x00000800      /* AMD: SSE5 */
#define CPUID_AMD_ECX_SKINIT    0x00001000      /* AMD: SKINIT */
#define CPUID_AMD_ECX_WDT       0x00002000      /* AMD: WDT */
#define CPUID_AMD_ECX_TOPOEXT   0x00400000      /* AMD: Topology Extensions */

#define FMT_CPUID_AMD_ECX                                           \
        "\20"                                                       \
        "\27topoext"                                                \
        "\16wdt\15skinit\14sse5\13ibs\12osvw\0113dnp\10mas"         \
        "\22topoext"                                                \
        "\14wdt\13skinit\12sse5\11ibs\10osvw\93dnp\8mas"            \
        "\7sse4a\6lzcnt\5cr8d\3svm\2lcmplgcy\1ahf64"

/*
 * Intel now seems to have claimed part of the "extended" function
 * space that we previously for non-Intel implementors to use.
 * More excitingly still, they've claimed bit 20 to mean LAHF/SAHF
 * is available in long mode i.e. what AMD indicate using bit 0.
 * On the other hand, everything else is labelled as reserved.
 */
#define CPUID_INTC_ECX_AHF64    0x00100000      /* LAHF and SAHF in long mode */

/*
 * Intel also uses cpuid leaf 7 to have additional instructions and features.
 * Like some other leaves, but unlike the current ones we care about, it
 * requires us to specify both a leaf in %eax and a sub-leaf in %ecx. To deal
 * with the potential use of additional sub-leaves in the future, we now
 * specifically label the EBX features with their leaf and sub-leaf.
 */
#define CPUID_INTC_EBX_7_0_BMI1         0x00000008      /* BMI1 instrs */
#define CPUID_INTC_EBX_7_0_AVX2         0x00000020      /* AVX2 supported */
#define CPUID_INTC_EBX_7_0_SMEP         0x00000080      /* SMEP in CR4 */
#define CPUID_INTC_EBX_7_0_BMI2         0x00000100      /* BMI2 Instrs */

#define P5_MCHADDR      0x0
#define P5_CESR         0x11
#define P5_CTR0         0x12
#define P5_CTR1         0x13

#define K5_MCHADDR      0x0
#define K5_MCHTYPE      0x01
#define K5_TSC          0x10
#define K5_TR12         0x12

#define REG_PAT         0x277

#define REG_MC0_CTL             0x400
#define REG_MC5_MISC            0x417
#define REG_PERFCTR0            0xc1
#define REG_PERFCTR1            0xc2

#define REG_PERFEVNT0           0x186
#define REG_PERFEVNT1           0x187

#define REG_TSC                 0x10    /* timestamp counter */
#define REG_APIC_BASE_MSR       0x1b
#define REG_X2APIC_BASE_MSR     0x800   /* The MSR address offset of x2APIC */

#if !defined(__xpv)
/*
 * AMD C1E
 */
#define MSR_AMD_INT_PENDING_CMP_HALT    0xC0010055
#define AMD_ACTONCMPHALT_SHIFT  27
#define AMD_ACTONCMPHALT_MASK   3
```

```
258 #endif

260 #define MSR_DEBUGCTL            0x1d9

262 #define DEBUGCTL_LBR            0x01
263 #define DEBUGCTL_BTF            0x02

265 /* Intel P6, AMD */
266 #define MSR_LBR_FROM            0x1db
267 #define MSR_LBR_TO              0x1dc
268 #define MSR_LEX_FROM            0x1dd
269 #define MSR_LEX_TO              0x1de

271 /* Intel P4 (pre-Prescott, non P4 M) */
272 #define MSR_P4_LBSTK_TOS        0x1da
273 #define MSR_P4_LBSTK_0          0x1db
274 #define MSR_P4_LBSTK_1          0x1dc
275 #define MSR_P4_LBSTK_2          0x1dd
276 #define MSR_P4_LBSTK_3          0x1de

278 /* Intel Pentium M */
279 #define MSR_P6M_LBSTK_TOS       0x1c9
280 #define MSR_P6M_LBSTK_0         0x040
281 #define MSR_P6M_LBSTK_1         0x041
282 #define MSR_P6M_LBSTK_2         0x042
283 #define MSR_P6M_LBSTK_3         0x043
284 #define MSR_P6M_LBSTK_4         0x044
285 #define MSR_P6M_LBSTK_5         0x045
286 #define MSR_P6M_LBSTK_6         0x046
287 #define MSR_P6M_LBSTK_7         0x047

289 /* Intel P4 (Prescott) */
290 #define MSR_PRP4_LBSTK_TOS      0x1da
291 #define MSR_PRP4_LBSTK_FROM_0   0x680
292 #define MSR_PRP4_LBSTK_FROM_1   0x681
293 #define MSR_PRP4_LBSTK_FROM_2   0x682
294 #define MSR_PRP4_LBSTK_FROM_3   0x683
295 #define MSR_PRP4_LBSTK_FROM_4   0x684
296 #define MSR_PRP4_LBSTK_FROM_5   0x685
297 #define MSR_PRP4_LBSTK_FROM_6   0x686
298 #define MSR_PRP4_LBSTK_FROM_7   0x687
299 #define MSR_PRP4_LBSTK_FROM_8   0x688
300 #define MSR_PRP4_LBSTK_FROM_9   0x689
301 #define MSR_PRP4_LBSTK_FROM_10  0x68a
302 #define MSR_PRP4_LBSTK_FROM_11  0x68b
303 #define MSR_PRP4_LBSTK_FROM_12  0x68c
304 #define MSR_PRP4_LBSTK_FROM_13  0x68d
305 #define MSR_PRP4_LBSTK_FROM_14  0x68e
306 #define MSR_PRP4_LBSTK_FROM_15  0x68f
307 #define MSR_PRP4_LBSTK_TO_0     0x6c0
308 #define MSR_PRP4_LBSTK_TO_1     0x6c1
309 #define MSR_PRP4_LBSTK_TO_2     0x6c2
310 #define MSR_PRP4_LBSTK_TO_3     0x6c3
311 #define MSR_PRP4_LBSTK_TO_4     0x6c4
312 #define MSR_PRP4_LBSTK_TO_5     0x6c5
313 #define MSR_PRP4_LBSTK_TO_6     0x6c6
314 #define MSR_PRP4_LBSTK_TO_7     0x6c7
315 #define MSR_PRP4_LBSTK_TO_8     0x6c8
316 #define MSR_PRP4_LBSTK_TO_9     0x6c9
317 #define MSR_PRP4_LBSTK_TO_10    0x6ca
318 #define MSR_PRP4_LBSTK_TO_11    0x6cb
319 #define MSR_PRP4_LBSTK_TO_12    0x6cc
320 #define MSR_PRP4_LBSTK_TO_13    0x6cd
321 #define MSR_PRP4_LBSTK_TO_14    0x6ce
322 #define MSR_PRP4_LBSTK_TO_15    0x6cf
```



```
324 #define MCI_CTL_VALUE           0xffffffff

326 #define MTRR_TYPE_UC            0
327 #define MTRR_TYPE_WC            1
328 #define MTRR_TYPE_WT            4
329 #define MTRR_TYPE_WP            5
330 #define MTRR_TYPE_WB            6
331 #define MTRR_TYPE_UC_           7

333 /*
334  * For Solaris we set up the page attritubute table in the following way:
335  * PAT0 Write-Back
336  * PAT1 Write-Through
337  * PAT2 Unchacheable-
338  * PAT3 Uncacheable
339  * PAT4 Write-Back
340  * PAT5 Write-Through
341  * PAT6 Write-Combine
342  * PAT7 Uncacheable
343  * The only difference from h/w default is entry 6.
344  */
345 #define PAT_DEFAULT_ATTRIBUTE                   \
346         ((uint64_t)MTRR_TYPE_WB |               \
347         ((uint64_t)MTRR_TYPE_WT << 8) |         \
348         ((uint64_t)MTRR_TYPE_UC_ << 16) |       \
349         ((uint64_t)MTRR_TYPE_UC << 24) |        \
350         ((uint64_t)MTRR_TYPE_WB << 32) |        \
351         ((uint64_t)MTRR_TYPE_WT << 40) |        \
352         ((uint64_t)MTRR_TYPE_WC << 48) |        \
353         ((uint64_t)MTRR_TYPE_UC << 56))

355 #define X86FSET_LARGEPAGE       0
356 #define X86FSET_TSC             1
357 #define X86FSET_MSR             2
358 #define X86FSET_MTRR            3
359 #define X86FSET_PGE             4
360 #define X86FSET_DE              5
361 #define X86FSET_CMOV            6
362 #define X86FSET_MMX             7
363 #define X86FSET_MCA             8
364 #define X86FSET_PAE             9
365 #define X86FSET_CX8             10
366 #define X86FSET_PAT             11
367 #define X86FSET_SEP             12
368 #define X86FSET_SSE             13
369 #define X86FSET_SSE2            14
370 #define X86FSET_HTT             15
371 #define X86FSET_ASYSC           16
372 #define X86FSET_NX              17
373 #define X86FSET_SSE3            18
374 #define X86FSET_CX16            19
375 #define X86FSET_CMP             20
376 #define X86FSET_TSCP            21
377 #define X86FSET_MWAIT           22
378 #define X86FSET_SSE4A           23
379 #define X86FSET_CPUID           24
380 #define X86FSET_SSSE3           25
381 #define X86FSET_SSE4_1          26
382 #define X86FSET_SSE4_2          27
383 #define X86FSET_1GPG            28
384 #define X86FSET_CLFSH           29
385 #define X86FSET_64              30
386 #define X86FSET_AES             31
387 #define X86FSET_PCLMULQDQ       32
388 #define X86FSET_XSAVE           33
389 #define X86FSET_AVX             34
```

```
390 #define X86FSET_VMX             35
391 #define X86FSET_SVM             36
392 #define X86FSET_TOPOEXT         37
393 #define X86FSET_F16C            38
394 #define X86FSET_RDRAND          39
395 #define X86FSET_X2APIC          40
396 #define X86FSET_AVX2            41
397 #define X86FSET_BMI1            42
398 #define X86FSET_BMI2            43
399 #define X86FSET_FMA             44
400 #define X86FSET_SMEP            45

402 /*
403  * flags to patch tsc_read routine.
404  */
405 #define X86_NO_TSC              0x0
406 #define X86_HAVE_TSCP           0x1
407 #define X86_TSC_MFENCE          0x2
408 #define X86_TSC_LFENCE          0x4

410 /*
411  * Intel Deep C-State invariant TSC in leaf 0x80000007.
412  */
413 #define CPUID_TSC_CSTATE_INVARIANCE     (0x100)

415 /*
416  * Intel Deep C-state always-running local APIC timer
417  */
418 #define CPUID_CSTATE_ARAT       (0x4)

420 /*
421  * Intel ENERGY_PERF_BIAS MSR indicated by feature bit CPUID.6.ECX[3].
422  */
423 #define CPUID_EPB_SUPPORT       (1 << 3)

425 /*
426  * Intel TSC deadline timer
427  */
428 #define CPUID_DEADLINE_TSC      (1 << 24)

430 /*
431  * x86_type is a legacy concept; this is supplanted
432  * for most purposes by x86_featureset; modern CPUs
433  * should be X86_TYPE_OTHER
434  */
435 #define X86_TYPE_OTHER          0
436 #define X86_TYPE_486            1
437 #define X86_TYPE_P5             2
438 #define X86_TYPE_P6             3
439 #define X86_TYPE_CYRIX_486      4
440 #define X86_TYPE_CYRIX_6x86L    5
441 #define X86_TYPE_CYRIX_6x86     6
442 #define X86_TYPE_CYRIX_GXm      7
443 #define X86_TYPE_CYRIX_6x86MX   8
444 #define X86_TYPE_CYRIX_MediaGX  9
445 #define X86_TYPE_CYRIX_MII      10
446 #define X86_TYPE_VIA_CYRIX_III  11
447 #define X86_TYPE_P4             12

449 /*
450  * x86_vendor allows us to select between
451  * implementation features and helps guide
452  * the interpretation of the cpuid instruction.
453  */
454 #define X86_VENDOR_Intel        0
455 #define X86_VENDORSTR_Intel     "GenuineIntel"
```



```
457 #define X86_VENDOR_IntelClone   1

459 #define X86_VENDOR_AMD          2
460 #define X86_VENDORSTR_AMD       "AuthenticAMD"

462 #define X86_VENDOR_Cyrix        3
463 #define X86_VENDORSTR_CYRIX     "CyrixInstead"

465 #define X86_VENDOR_UMC          4
466 #define X86_VENDORSTR_UMC       "UMC UMC UMC "

468 #define X86_VENDOR_NexGen       5
469 #define X86_VENDORSTR_NexGen    "NexGenDriven"

471 #define X86_VENDOR_Centaur      6
472 #define X86_VENDORSTR_Centaur   "CentaurHauls"

474 #define X86_VENDOR_Rise         7
475 #define X86_VENDORSTR_Rise      "RiseRiseRise"

477 #define X86_VENDOR_SiS          8
478 #define X86_VENDORSTR_SiS       "SiS SiS SiS "

480 #define X86_VENDOR_TM           9
481 #define X86_VENDORSTR_TM        "GenuineTMx86"

483 #define X86_VENDOR_NSC          10
484 #define X86_VENDORSTR_NSC       "Geode by NSC"

486 /*
487  * Vendor string max len + \0
488  */
489 #define X86_VENDOR_STRLEN       13

491 /*
492  * Some vendor/family/model/stepping ranges are commonly grouped under
493  * a single identifying banner by the vendor.  The following encode
494  * that "revision" in a uint32_t with the 8 most significant bits
495  * identifying the vendor with X86_VENDOR_*, the next 8 identifying the
496  * family, and the remaining 16 typically forming a bitmask of revisions
497  * within that family with more significant bits indicating "later" revisions.
498  */

500 #define _X86_CHIPREV_VENDOR_MASK        0xff000000u
501 #define _X86_CHIPREV_VENDOR_SHIFT       24
502 #define _X86_CHIPREV_FAMILY_MASK        0x00ff0000u
503 #define _X86_CHIPREV_FAMILY_SHIFT       16
504 #define _X86_CHIPREV_REV_MASK           0x0000ffffu

506 #define _X86_CHIPREV_VENDOR(x) \
507         (((x) & _X86_CHIPREV_VENDOR_MASK) >> _X86_CHIPREV_VENDOR_SHIFT)
508 #define _X86_CHIPREV_FAMILY(x) \
509         (((x) & _X86_CHIPREV_FAMILY_MASK) >> _X86_CHIPREV_FAMILY_SHIFT)
510 #define _X86_CHIPREV_REV(x) \
511         ((x) & _X86_CHIPREV_REV_MASK)

513 /* True if x matches in vendor and family and if x matches the given rev mask */
514 #define X86_CHIPREV_MATCH(x, mask) \
515         (_X86_CHIPREV_VENDOR(x) == _X86_CHIPREV_VENDOR(mask) && \
516         _X86_CHIPREV_FAMILY(x) == _X86_CHIPREV_FAMILY(mask) && \
517         ((_X86_CHIPREV_REV(x) & _X86_CHIPREV_REV(mask)) != 0))

519 /* True if x matches in vendor and family, and rev is at least minx */
520 #define X86_CHIPREV_ATLEAST(x, minx) \
521         (_X86_CHIPREV_VENDOR(x) == _X86_CHIPREV_VENDOR(minx) && \
```

```
522         _X86_CHIPREV_FAMILY(x) == _X86_CHIPREV_FAMILY(minx) && \
523         _X86_CHIPREV_REV(x) >= _X86_CHIPREV_REV(minx))

525 #define _X86_CHIPREV_MKREV(vendor, family, rev) \
526         ((uint32_t)(vendor) << _X86_CHIPREV_VENDOR_SHIFT | \
527         (family) << _X86_CHIPREV_FAMILY_SHIFT | (rev))

529 /* True if x matches in vendor, and family is at least minx */
530 #define X86_CHIPFAM_ATLEAST(x, minx) \
531         (_X86_CHIPREV_VENDOR(x) == _X86_CHIPREV_VENDOR(minx) && \
532         _X86_CHIPREV_FAMILY(x) >= _X86_CHIPREV_FAMILY(minx))

534 /* Revision default */
535 #define X86_CHIPREV_UNKNOWN     0x0

537 /*
538  * Definitions for AMD Family 0xf. Minor revisions C0 and CG are
539  * sufficiently different that we will distinguish them; in all other
540  * case we will identify the major revision.
541  */
542 #define X86_CHIPREV_AMD_F_REV_B _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0001)
543 #define X86_CHIPREV_AMD_F_REV_C0 _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0002)
544 #define X86_CHIPREV_AMD_F_REV_CG _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0004)
545 #define X86_CHIPREV_AMD_F_REV_D _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0008)
546 #define X86_CHIPREV_AMD_F_REV_E _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0010)
547 #define X86_CHIPREV_AMD_F_REV_F _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0020)
548 #define X86_CHIPREV_AMD_F_REV_G _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0xf, 0x0040)

550 /*
551  * Definitions for AMD Family 0x10.  Rev A was Engineering Samples only.
552  */
553 #define X86_CHIPREV_AMD_10_REV_A \
554         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0001)
555 #define X86_CHIPREV_AMD_10_REV_B \
556         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0002)
557 #define X86_CHIPREV_AMD_10_REV_C2 \
558         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0004)
559 #define X86_CHIPREV_AMD_10_REV_C3 \
560         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0008)
561 #define X86_CHIPREV_AMD_10_REV_D0 \
562         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0010)
563 #define X86_CHIPREV_AMD_10_REV_D1 \
564         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0020)
565 #define X86_CHIPREV_AMD_10_REV_E \
566         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x10, 0x0040)

568 /*
569  * Definitions for AMD Family 0x11.
570  */
571 #define X86_CHIPREV_AMD_11_REV_B \
572         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x11, 0x0002)

574 /*
575  * Definitions for AMD Family 0x12.
576  */
577 #define X86_CHIPREV_AMD_12_REV_B \
578         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x12, 0x0002)

580 /*
581  * Definitions for AMD Family 0x14.
582  */
583 #define X86_CHIPREV_AMD_14_REV_B \
584         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x14, 0x0002)
585 #define X86_CHIPREV_AMD_14_REV_C \
586         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x14, 0x0004)
```



```
588 /*
589  * Definitions for AMD Family 0x15
590  */
591 #define X86_CHIPREV_AMD_15OR_REV_B2 \
592         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x15, 0x0001)

594 #define X86_CHIPREV_AMD_15TN_REV_A1 \
595         _X86_CHIPREV_MKREV(X86_VENDOR_AMD, 0x15, 0x0002)

597 /*
598  * Various socket/package types, extended as the need to distinguish
599  * a new type arises.  The top 8 byte identfies the vendor and the
600  * remaining 24 bits describe 24 socket types.
601  */

603 #define _X86_SOCKET_VENDOR_SHIFT        24
604 #define _X86_SOCKET_VENDOR(x)   ((x) >> _X86_SOCKET_VENDOR_SHIFT)
605 #define _X86_SOCKET_TYPE_MASK   0x00ffffff
606 #define _X86_SOCKET_TYPE(x)             ((x) & _X86_SOCKET_TYPE_MASK)

608 #define _X86_SOCKET_MKVAL(vendor, bitval) \
609         ((uint32_t)(vendor) << _X86_SOCKET_VENDOR_SHIFT | (bitval))

611 #define X86_SOCKET_MATCH(s, mask) \
612         (_X86_SOCKET_VENDOR(s) == _X86_SOCKET_VENDOR(mask) && \
613         (_X86_SOCKET_TYPE(s) & _X86_SOCKET_TYPE(mask)) != 0)

615 #define X86_SOCKET_UNKNOWN 0x0
616         /*
617          * AMD socket types
618          */
619 #define X86_SOCKET_754          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000001)
620 #define X86_SOCKET_939          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000002)
621 #define X86_SOCKET_940          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000004)
622 #define X86_SOCKET_S1g1         _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000008)
623 #define X86_SOCKET_AM2          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000010)
624 #define X86_SOCKET_F1207        _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000020)
625 #define X86_SOCKET_S1g2         _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000040)
626 #define X86_SOCKET_S1g3         _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000080)
627 #define X86_SOCKET_AM           _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000100)
628 #define X86_SOCKET_AM2R2        _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000200)
629 #define X86_SOCKET_AM3          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000400)
630 #define X86_SOCKET_G34          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x000800)
631 #define X86_SOCKET_ASB2         _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x001000)
632 #define X86_SOCKET_C32          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x002000)
633 #define X86_SOCKET_S1g4         _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x004000)
634 #define X86_SOCKET_FT1          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x008000)
635 #define X86_SOCKET_FM1          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x010000)
636 #define X86_SOCKET_FS1          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x020000)
637 #define X86_SOCKET_AM3R2        _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x040000)
638 #define X86_SOCKET_FP2          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x080000)
639 #define X86_SOCKET_FS1R2        _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x100000)
640 #define X86_SOCKET_FM2          _X86_SOCKET_MKVAL(X86_VENDOR_AMD, 0x200000)

642 /*
643  * xgetbv/xsetbv support
644  */

646 #define XFEATURE_ENABLED_MASK   0x0
647 /*
648  * XFEATURE_ENABLED_MASK values (eax)
649  */
650 #define XFEATURE_LEGACY_FP      0x1
651 #define XFEATURE_SSE            0x2
652 #define XFEATURE_AVX            0x4
653 #define XFEATURE_MAX            XFEATURE_AVX
```

```
 654 #define XFEATURE_FP_ALL \
 655         (XFEATURE_LEGACY_FP|XFEATURE_SSE|XFEATURE_AVX)

 657 #if !defined(_ASM)

 659 #if defined(_KERNEL) || defined(_KMEMUSER)

 661 #define NUM_X86_FEATURES        46
 662 extern uchar_t x86_featureset[];

 664 extern void free_x86_featureset(void *featureset);
 665 extern boolean_t is_x86_feature(void *featureset, uint_t feature);
 666 extern void add_x86_feature(void *featureset, uint_t feature);
 667 extern void remove_x86_feature(void *featureset, uint_t feature);
 668 extern boolean_t compare_x86_featureset(void *setA, void *setB);
 669 extern void print_x86_featureset(void *featureset);


 672 extern uint_t x86_type;
 673 extern uint_t x86_vendor;
 674 extern uint_t x86_clflush_size;

 676 extern uint_t pentiumpro_bug4046376;

 678 extern const char CyrixInstead[];

 680 #endif

 682 #if defined(_KERNEL)

 684 /*
 685  * This structure is used to pass arguments and get return values back
 686  * from the CPUID instruction in __cpuid_insn() routine.
 687  */
 688 struct cpuid_regs {
 689         uint32_t        cp_eax;
 690         uint32_t        cp_ebx;
 691         uint32_t        cp_ecx;
 692         uint32_t        cp_edx;
 693 };
```

_____***unchanged_portion_omitted_***